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Description

[SEMICONDUCTOR DEVICE]

BACKGROUND OF INVENTION

[0001] *Field of the Present Invention*

[0002] The present invention relates to a semiconductor device and, more specifically, relates to a DCS (Dual Chip Stack) semiconductor device.

[0003] *Description of Related Art*

[0004] Semiconductor devices are often employed in FPGA (Fine Pitch ball Grid Array) systems and so forth. Fig. 7 (Prior Art) is a sectional view showing a structure of a conventional DCS semiconductor device.

[0005] Referring to Fig. 7, the DCS semiconductor device 1 comprises a substrate 11, a bottom semiconductor chip 12 including an electrical circuit (not shown) such as an SRAM (Static Random Access Memory), and a top semiconductor chip 13 including an electrical circuit (not shown) such as a flash memory. The bottom semiconductor chip 12 is mounted on the substrate 11 using adhesive paste 14.

The top semiconductor chip 13 is mounted on the bottom semiconductor chip 12 using adhesive paste 15. Further, resin 16 is molded on the substrate 11 so as to cover the bottom semiconductor chip 12 and the top semiconductor chip 13.

[0006] In the conventional DCS semiconductor device 1, inasmuch as the sizes of the bottom semiconductor chip 12 and the top semiconductor chip 13 are equal to each other, even if these chips are subjected to thermal expansion in the molding process of the resin 16, stresses to be generated therein will be equal to each other. Therefore, the thermal expansion of the semiconductor chips 12 and 13 does not cause warping of the DCS semiconductor device 1. On the other hand, since the thermal expansion coefficient of the resin 16 differs from that of the semiconductor chips 12 and 13, and the resin 16 may also be contracted, this may cause warping of the DCS semiconductor device 1 as shown in Fig. 8 (Prior Art). However, even if it is warped, the warping amounts of the bottom semiconductor chip 12 and the top semiconductor chip 13 are substantially the same. Therefore, it is unlikely that stresses are generated concentratedly in the DCS semiconductor device 1.

[0007] As described above, the size of the top semiconductor chip 13 is the same as that of the bottom semiconductor chip 12 in the conventional DCS semiconductor device 1. However, as shown in Fig. 9, it is hereby assumed that a DCS semiconductor device 2 employs, instead of the top semiconductor chip 13, a top semiconductor chip 21 having a size smaller than that of the bottom semiconductor chip 12. As appreciated, this DCS semiconductor device 2 is only for explaining a theme of the present invention, and does not constitute the prior art.

[0008] In the DCS semiconductor device 2, resin 16 is filled in the portion where the top semiconductor chip 13 is provided in the conventional DCS semiconductor device 1. Inasmuch as the thermal expansion coefficient of the resin 16 largely differs from that of the semiconductor chips 12 and 21, the DCS semiconductor device 2 tends to be warped as shown in Fig. 10. Moreover, inasmuch as the size of the top semiconductor chip 21 is smaller than that of the bottom semiconductor chip 12, warping of the bottom semiconductor chip 12 becomes greater than that of the top semiconductor chip 21. Therefore, stresses are concentrated in the neighborhood of portions where edges 211 of a lower surface of the top semiconductor

chip 21 contact an upper surface of the bottom semiconductor chip 12 and in the neighborhood of portions where edges 121 of a lower surface of the bottom semiconductor chip 12 contact an upper surface of a substrate 11. As a result, there is a possibility that the upper surfaces of the bottom semiconductor chip 12 and the substrate 11 may be damaged. This problem becomes more significant as the position of the top semiconductor chip 21 approaches an end of the bottom semiconductor chip 12 as compared with being located at the center thereof. This is because stresses are generated asymmetrically.

[0009] As one method of solving such a problem, it is considered that adhesive pastes 14 and 15 may be applied thicker. However, there is a possibility that a steam explosion phenomenon may occur in the adhesive pastes 14 and 15 upon reflow-soldering the DCS semiconductor device 2 to a printed circuit board or the like.

[0010] It would, therefore, be a distinct advantage to have a semiconductor device that can suppress damage to an internal semiconductor chip caused by a stress produced by warping of the semiconductor device. The present invention provides such a semiconductor device.

SUMMARY OF INVENTION

[0011] In one aspect, the present invention is a semiconductor device includes a substrate, a first semiconductor chip, and a second semiconductor chip. The first semiconductor chip is mounted on the substrate. The second semiconductor chip is mounted on the first semiconductor chip, and is smaller in size and thickness than the first semiconductor chip.

[0012] The second semiconductor chip being smaller in size than the first semiconductor chip, but the first semiconductor chip is thicker than the second semiconductor chip. Accordingly, even if the semiconductor device is warped, stresses are reluctant to occur concentratedly. Therefore, damage to the first semiconductor chip caused by the second semiconductor chip can be suppressed.

[0013] In yet another aspect, the present invention is a r semiconductor device having a substrate, a first semiconductor chip, and a second semiconductor chip. The first semiconductor chip is mounted on the substrate. The second semiconductor chip is mounted on the first semiconductor chip, and is smaller in size than the first semiconductor chip. An edge of a lower surface of the second semiconductor chip confronting an upper surface of the first semiconductor chip is chamfered.

[0014] The second semiconductor chip is smaller in size than the first semiconductor chip, but the edge of the lower surface of the second semiconductor chip is chamfered. Accordingly, even if the semiconductor device is warped, stresses are reluctant to occur concentratedly. Therefore, damage to the first semiconductor chip caused by the second semiconductor chip can be suppressed.

Brief Description of Drawings

[0015] Fig. 1 is a plan view showing an external appearance of a DCS semiconductor device according to a first preferred embodiment of the present invention.

[0016] Fig. 2 is a sectional view of the DCS semiconductor device, taken along line I-II in Fig. 1.

[0017] Fig. 3 is a graph showing variation of distortion when the size and thickness of a bottom semiconductor chip are changed while keeping constant the size and thickness of a top semiconductor chip in the DCS semiconductor device shown in Fig. 1.

[0018] Fig. 4 is a graph wherein the size and thickness of the bottom semiconductor chip shown in Fig. 3 are converted into the ratios thereof relative to the size and thickness of the top semiconductor chip.

[0019] Fig. 5 is a sectional view showing a structure of a DCS

semiconductor device according to a second preferred embodiment of the present invention.

[0020] Fig. 6 is a sectional view exemplarily showing the state wherein the DCS semiconductor device shown in Fig. 5 is warped.

[0021] Fig. 7 is a sectional view showing a structure of a conventional DCS semiconductor device.

[0022] Fig. 8 is a sectional view exemplarily showing the state wherein the DCS semiconductor device shown in Fig. 7 is warped.

[0023] Fig. 9 is a sectional view showing a structure of a DCS semiconductor device that is assumed when a top semiconductor chip is made smaller in size than a bottom semiconductor chip.

[0024] Fig. 10 is a sectional view exemplarily showing the state wherein the DCS semiconductor device shown in Fig. 9 is warped.

DETAILED DESCRIPTION

[0025] Hereinbelow, preferred embodiments of the present invention will be described in detail with reference to the drawings. In the drawings, the same or corresponding portions are assigned the same reference symbols to thereby incorporate the description thereof.

[0026] First Preferred Embodiment

[0027] Fig. 1 is a plan view showing an external appearance of a DCS semiconductor device according to the first preferred embodiment of the present invention. Fig. 2 is a sectional view taken along line I-II in Fig. 1.

[0028] Referring to Figs. 1 and 2, this DCS semiconductor device 3 comprises a substrate 11 made of glass epoxy resin or the like, a bottom semiconductor chip 31 including a predetermined electrical circuit (not shown), and a top semiconductor chip 32 including a predetermined electrical circuit (not shown). As a combination of the electrical circuit included in the bottom semiconductor chip 31 and the electrical circuit included in the top semiconductor chip 32, there can be cited, for example, a logic circuit and an analog circuit, a logic circuit and a memory, or the like.

[0029] The bottom semiconductor chip 31 is mounted on the substrate 11 using adhesive paste 14. The top semiconductor chip 32 is mounted on the bottom semiconductor chip 31 using adhesive paste 15. The bottom semiconductor chip 31 is electrically connected to the substrate 11 using wire bonding. The top semiconductor chip 32 is electrically connected to the bottom semiconductor chip

31 and the substrate 11 using wire bonding. Because of the limitation on the wire bonding length, the top semiconductor chip 32 is mounted on the bottom semiconductor chip 31 near an end thereof, rather than at the center thereof.

[0030] Further, resin 16 is molded on the substrate 11 so as to cover the bottom semiconductor chip 31 and the top semiconductor chip 32.

[0031] The DCS semiconductor device 3 differs from the foregoing conventional DCS semiconductor device 1 in that the size of the top semiconductor chip 32 is smaller than that of the bottom semiconductor chip 31, and a thickness t3 of the bottom semiconductor chip 31 is greater than a thickness t5 of the top semiconductor chip 32. The sizes of the bottom semiconductor chip 31 and the top semiconductor chip 32 are not particularly limited, but there can be cited, as an example, a combination of 6mm square (6mm x 6mm) and 3.5mm x 1.5mm.

[0032] The thickness t3 of the bottom semiconductor chip 31 is maximized while the thickness t5 of the top semiconductor chip 32 is minimized, so as to be received in a thickness t7 of the resin 16. Specifically, assuming that the thickness t7 of the resin 16 is 0.700mm, inasmuch as it is

necessary to ensure 0.040mm for each thicknesses t2 and t4 of the adhesive pastes 14 and 15 and 0.150mm for a thickness t6 of an upper space over the top semiconductor chip 32, the thicknesses t3 and t5 of the bottom semiconductor chip 31 and the top semiconductor chip 32 are respectively set to, for example, 0.300mm and 0.150mm, or 0.350mm and 0.100mm.

[0033] A thickness t1 of the substrate 11 is also not particularly limited, but there can be cited, as an example, 0.21mm, 0.26mm, 0.32mm, or the like.

[0034] Fig. 3 is a graph showing the relation between the thickness t3 of the bottom semiconductor chip 31 and distortion thereof per size of the bottom semiconductor chip 31. The axis of abscissas represents the thickness t3 (mm) of the bottom semiconductor chip 31, while the axis of ordinates represents the magnitude of distortion (arbitrary unit) at a portion where stresses are concentrated most. With respect to the size of the bottom semiconductor chip 31, represents 10mm square, 8mm square, 6mm square, x 4mm square, and * 2.5mm square. By fixing the size of the top semiconductor chip 32 to 2mm square and the thickness t5 thereof to 0.100mm, and changing the size of the bottom semicon-

ductor chip 31 from 10.0mm square to 2.5mm square, and the thickness t3 thereof from 0.100mm to 0.500mm, the relations shown in the graph of Fig. 3 are obtained.

[0035] Fig. 4 is a graph wherein the sizes and thicknesses shown in fig. 3 are converted into the ratios. The axis of abscissas represents the ratio of the thickness t3 of the bottom semiconductor chip 31 relative to the thickness t5 of the top semiconductor chip 32. With respect to the ratio of the size of the bottom semiconductor chip 31 relative to the size of the top semiconductor chip 32, represents 5.0, 4.0, 3.0, x 2.0 and * 1.5. Since the ratio of areas is the square of the ratio of sizes, when the ratio of sizes is converted into the ratio or areas, represents 25.0, 16.0, 9.0, x 4.0, and * 2.25.

[0036] As clearly seen from Figs. 3 and 4, the distortion increases as the ratio of the thickness t3 of the bottom semiconductor chip 31 relative to the thickness t5 of the top semiconductor chip 32 decreases. This relationship becomes more outstanding as the ratio of the size of the bottom semiconductor chip 31 relative to the size of the top semiconductor chip 32 increases. In other words, as the ratio of an area of the top semiconductor chip 32 occupying an area of the bottom semiconductor chip 31 in-

creases, the thickness t3 of the bottom semiconductor chip 31 largely affects the distortion.

[0037] Therefore, as the thickness t3 of the bottom semiconductor chip 31 is increased relative to the thickness t5 of the top semiconductor chip 32, the distortion becomes smaller. For example, assuming that the ratio of the size of the bottom semiconductor chip 31 relative to the size of the top semiconductor chip 32 is 5.0 (in case of Fig. 4), the distortion becomes maximum when the thicknesses t3 and t5 of the bottom semiconductor chip 31 and the top semiconductor chip 32 are both 0.100mm, while, when the thickness t3 of the bottom semiconductor chip 31 is 0.500mm (5.0 times the thickness t5 of the top semiconductor chip 32), the distortion is reduced to 6.7% of the maximum. Further, for example, assuming that the ratio of the size of the bottom semiconductor chip 31 relative to the size of the top semiconductor chip 32 is 2.0 (in case of x in Fig. 4), when the thickness t3 of the bottom semiconductor chip 31 becomes 0.120mm or more (no less than 1.2 times the thickness t5 of the top semiconductor chip 32), the distortion becomes smaller than 50.0, i.e. the distortion is reduced to about 80% of the maximum. Accordingly, when the size of the bottom semicon-

ductor chip 31 becomes no less than twice the size of the top semiconductor chip 32, the distortion is further reduced.

[0038] As described above, according to the first preferred embodiment, when the top semiconductor chip 32 is smaller than the bottom semiconductor chip 31, the bottom semiconductor chip 31 is made thicker than the top semiconductor chip 32, so that even if the semiconductor device 3 is warped, generated stresses can be reduced. As a result, damage to the bottom semiconductor chip 31 and the substrate 11 can be suppressed to a smaller degree.

[0039] Second Preferred Embodiment

[0040] In the foregoing first preferred embodiment, when the size of the top semiconductor chip 32 is smaller than that of the bottom semiconductor chip 31, the thickness of the bottom semiconductor chip 31 is maximized while the thickness of the top semiconductor chip 32 is minimized within the allowable range in terms of the reception of them in the resin 16, for the purpose of reducing the concentrated stresses generated by the warping. On the other hand, in the second preferred embodiment, as shown in Fig. 5, edges 411 and 412 of a lower surface of a top semiconductor chip 41 confronting an upper surface of a

bottom semiconductor chip 12 are chamfered.

[0041] The top semiconductor chip 41 is generally produced via a dicing process wherein a large plate is cut into strips, and therefore, the foregoing chamfering may be carried out by bevel dicing in the dicing process. The top semiconductor chip 41 has a rectangular parallelepiped shape, and thus has four sides on the lower surface thereof. The chamfering is preferably applied to all the four sides, but may be applied to at least one of the sides where the concentrated stresses are maximized. In case of a semiconductor device 4 shown in Fig. 5, it is sufficient to apply the chamfering to the edge 411 located closer to the center of the bottom semiconductor chip 12. A chamfering width C is not particularly limited. However, when the thickness of the top semiconductor chip 41 is 0.150mm, it is set to, for example, 0.050mm to 0.100mm.

[0042] Even if the semiconductor device 4 is warped as shown in Fig. 6, inasmuch as the edges 411 and 412 of the lower surface of the top re chamfered, the stresses are concentrated on the edges 411 and 412 so that no damage is given to the bottom semiconductor chip 12.

[0043] In this embodiment, the thickness of the top semiconductor chip 41 is equal to that of the bottom semiconductor

chip 12. However, like in the foregoing first preferred embodiment, the thickness of the top semiconductor chip 41 may be set smaller than that of the bottom semiconductor chip 12. That is, the foregoing first preferred embodiment and this second preferred embodiment may be combined together. In this case, the concentrated stresses can be further reduced to thereby further reduce the damage to the bottom semiconductor chip 12 and the substrate 11.

[0044] *Another Preferred Embodiment*

[0045] In the foregoing preferred embodiments, the top semiconductor chip is mounted near the end of the bottom semiconductor chip rather than at the center thereof, which, however, is not necessarily required, i.e. the top semiconductor chip may be mounted at the center of the bottom semiconductor chip. Further, although two semiconductor chips are stacked together in the foregoing preferred embodiments, three or more semiconductor chips may be stacked together.

[0046] The description has been given above about the preferred embodiments of the present invention. However, the foregoing preferred embodiments are only the examples for carrying out the present invention. Therefore, the present invention is not limited to the foregoing preferred embod-

iments, but may be carried out by properly changing the foregoing preferred embodiments without departing from the gist of the present invention.